INFORMAL COMMUNICATION - DO NOT ENTER
Patent Application No.: 09/754,406

Filing Date: January 2, 2001
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Attorney Docket No.: APLUS.001A
Examiner: Tom Stevens
Art Unit: 2123

1. (Currently amended) A method of reducing circuit timing delays, comprising:

selecting a first node;

sorting fanins of the first node according to corresponding associated slack values ~~associated with the corresponding fanins~~, wherein at least a portion of the slack values differ in value; and

reducing delays, **via a delay reduction process,** associated with the sorted fanins having relatively larger negative slack values before reducing delays associated with the sorted fanins having relatively smaller negative slack values, wherein the delay reduction improves circuit performance.

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11. (Currently amended) A method of reducing timing delays for a circuit having primary input (PI) nodes, at least one primary output (PO) node, and a set of circuit nodes between the PI nodes and the PO node(s), the method comprising:

a) identifying a first critical path between a first PI node and a first PO node, wherein the first critical path is selected based on ordering the PO nodes by corresponding slack values;

b) beginning at the first PO node, attempting to reduce a delay associated with a first circuit node **via a delay reduction process**;

c) determining if the delay reduction meets a first predetermined criteria;

d) identifying a following circuit node in the critical path if the predetermined criteria is not met;

e) attempting to reduce a delay associated with the following circuit node to improve circuit performance;

f) repeating c), d) and e) until the delay cannot be reduced or a set of constraints are violated;

g) identifying a second critical path between a second PI node and a second PO node, wherein the second critical path is selected based on the ordered PO nodes;

h) determining an amount of delay reduction still needed for the second critical path after applying the results of the delay reduction for the first critical path; and

i) beginning at the second PO node, attempting to reduce a delay associated with a second circuit node to improve circuit performance.

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21. (Currently amended) A method of dynamically reducing delays on a critical path of a circuit topology, the method comprising:

identifying a critical path of the circuit topology;

selecting a delay target for a primary output associated with the critical path;

dynamically reducing a first critical path delay at a first node in closer proximity to a primary input associated with the critical path than to a node in closer proximity to the primary output;

storing the reduced delay; ~~and~~

recursively dynamically reducing a second critical path delay beginning at a second node located between the first node and the primary output **via a delay reduction process** based at least in part on the stored reduced delay; and

storing/saving the reduced second path delay time.

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